DATA SHEET

TDA9888TS; TDA9889TS
DVB selective AGC amplifier

Product specification

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Philips
Semiconductors

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FEATURES

- Applicable for terrestrial and cable TV reception
- 70 dB variable gain wide-band Intermediate Frequency (IF) amplifier (AC-coupled)
- Gain control via external control voltage (0 to 3 V)
- 2 V (p-p) differential low IF (downconverted) output for direct Analog-to-Digital Converter (ADC) interfacing
- Digital Video Broadcast (DVB) downconversion with integrated selectivity (allows to use one SAW filter applications)
- Integrated anti-aliasing tracking low-pass filter
- Fully integrated synthesizer controlled oscillator with excellent phase noise performance
- Synthesizer frequencies for a wide range of world wide DVB standards (for IF centre frequencies of 36, 44 and 57 MHz) with different channel bandwidths (6, 7 and 8 MHz) are possible; see Tables 1 and 2
- 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
- Tuner Automatic Gain Control (TAGC) detector for independent tuner gain control loop applications
- TAGC operating as peak-sync detector, fast reaction time due to additional speed-up detector
- TAGC switch for feed-through of TAGC signal from analog TV demodulator (e.g. TDA9886) in case of hybrid (analog and digital TV demodulation) application
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- Electrostatic discharge (ESD) protection for all pins.

GENERAL DESCRIPTION

The TDA9888TS; TDA9889TS is an AGC amplifier circuit with integrated selectivity. The device provides downconversion and filtering without alignment for all DVB standards. The filtering considers the tough neighbouring channel conditions.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9888TS	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
TDA9889TS			

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		46	55	64	mA
$V_{o(LIF)(p-p)}$	typical low IF operating output voltage (peak-to-peak value)		–	2	–	V
$G_{IF(max)}$	maximum conversion gain	output peak-to-peak level to input RMS level ratio	85	90	–	dB
$G_{IF(cr)}$	IF gain control range	see Fig.3	60	70	–	dB
f_{osc}	synthesizer controlled oscillator frequencies	see Tables 1 and 2	–	31	–	MHz
			–	31.5	–	MHz
			–	32	–	MHz
			–	40	–	MHz
			–	53	–	MHz
$\phi_{N(synth)}$	synthesizer phase noise performance	at 1 kHz	89	99	–	dBc
		at 10 kHz	89	97	–	dBc
		at 100 kHz	98	102	–	dBc
α_{LIF}	low IF band amplitude characteristic	0 dB at middle of band (standard independent)	–0.9	–	+0.9	dB
α_{N-1}	low-pass filter attenuation	8 MHz band; at 15.75 MHz	15	–	–	dB
α_{N+1}	suppression of IF input frequencies below wanted band at low IF output	input frequency between 21 and 31 MHz; referenced to 36 MHz	30	–	–	dB
C/N	carrier-to-noise ratio at low IF	at Δf > 1 MHz; see Fig.5	112	116	–	dBc/Hz
PSRR	power supply ripple rejection [residual ripple AM, modulation factor m at 2 V (p-p) low IF signal]	f_{ripple} = 70 Hz; see Fig.7	–	1.4	–	%

Note

1. Some parameters can be decreased at V_P = 4.5 V.

BLOCK DIAGRAM

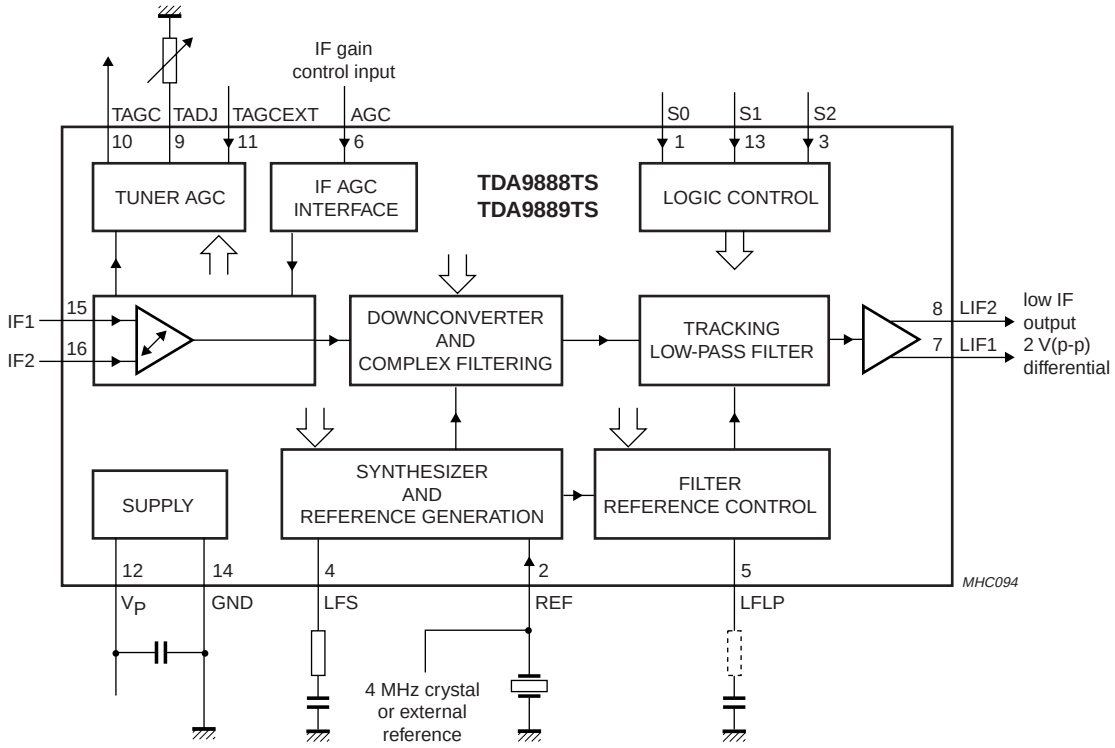


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S0	1	logic switch S0 input (frequency select)
REF	2	4 MHz crystal or reference input
S2	3	logic switch S2 input (AGC select)
LFS	4	loop filter synthesizer PLL
LFLP	5	loop filter low-pass control PLL
AGC	6	AGC control voltage input
LIF1	7	low IF differential output 1
LIF2	8	low IF differential output 2
TADJ	9	tuner AGC TakeOver Point (TOP) adjustment
TAGC	10	tuner AGC output
TAGCEXT	11	external tuner AGC voltage input
V_P	12	supply voltage (+5 V)
S1	13	logic switch S1 input (frequency select)
GND	14	ground supply
IF1	15	IF differential input 1
IF2	16	IF differential input 2

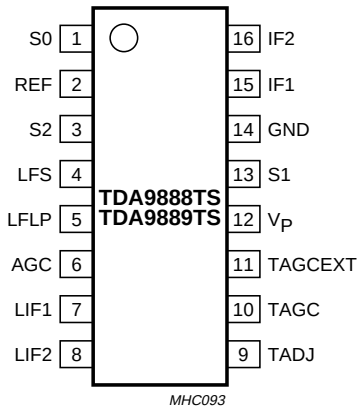


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 shows the simplified block diagram of the device. The integrated circuit contains the following functional blocks:

1. Gain controlled IF amplifier
2. Tuner AGC
3. Reference generation
4. Synthesizer for downconversion
5. Downconversion and complex filtering
6. Tracking low-pass filter with reference control
7. Low IF differential output stage
8. Logic control
9. Internal voltage stabilizer.

Gain controlled IF amplifier

The IF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. Total gain control range is 70 dB (typ.). The differential input impedance is typical 2 kΩ in parallel with 3 pF.

Tuner AGC

The tuner AGC is realized by a TakeOver Point (TOP) network and a peak-level detector. The threshold level of the peak detector can be adjusted by an external potentiometer connected to pin TADJ. For IF signals above this threshold the level detector provides a discharge current to pin TAGC. An additional current source is internally connected to this pin providing charge current to the external tuner AGC capacitor. For IF signals of 8 dB below the threshold voltage this current will be increased by a factor of approximately 40 for faster AGC reaction. The ratio of discharge to charge current is normally approximately 2000 and approximately 50 for fast mode.

For use of the device in different applications the charge current can be switched off, for hybrid applications the signal at pin TAGCEXT can be fed via a transmission gate to pin TAGC (TDA9888TS; TDA9889TS combined with analog IF), controlled by the 3-state input pin S2. With an activated transmission gate all internal currents are off. In the event that the tuner AGC is not needed (e.g. TAGC from channel decoder or from an analog IF in hybrid chassis), pin TADJ should be left open-circuit and therefore all internal AGC currents will be switched off.

Reference generation

The 4 MHz crystal is the reference for the downconversion synthesizer and the filter synthesizer.

The downconverted DVB frequency and the frequency adjustment of the integrated filters are dependent on the precision of the reference signal at pin REF. An operation as crystal oscillator is possible as well as connecting this input via a serial capacitor to another low-ohmic reference frequency source.

The integrated divider-by-8 generates the internally needed 500 kHz reference frequency for the DVB synthesizer and the reference filter.

Synthesizer for downconversion

The PLL synthesizer for downconversion consists of a Voltage Controlled Oscillator (VCO), a divider with a standard dependent divider factor, a frequency phase detector (constructed as a digital 3-state comparator) and a charge pump.

The VCO operates as an integrated low radiation relaxation oscillator at double the conversion frequency. For downconversion the VCO frequency is divided-by-2 to provide two differential square wave signals with exactly 90 degrees phase difference, independent of the VCO frequency.

The frequency phase detector compares the down-divided oscillator signal with the 500 kHz reference frequency signal and controls, via the charge pump, the control voltage at the external loop filter connected to pin LFS, which is required to tune the VCO exactly to the wanted frequency.

The divider, the frequency phase detector and the reference frequency divider are constructed in a low radiation technique to optimize the synthesizer spurious suppression in the downconverted output signal.

Downconversion and complex filtering

The gain controlled IF signal from the IF amplifier is fed to two identical linear mixers, operating in the ‘in phase’ and ‘quadrature’ mode in accordance to the 0 and 90 degree VCO signal from the synthesizer. With this, the downconverted DVB low IF signal is available as an I and Q signal in the frequency band from 1 to 9 MHz. These signals are fed to the complex filter section. As a result of adding both signals, the unwanted mirror signal will be attenuated (approximately 34 dB). The unwanted frequency components below 1 MHz are attenuated in a high-pass filter. This signal is then fed through a group-delay equalizer circuit.

Tracking low-pass filter with reference control

The low-pass filter is controlled by a reference signal [generated by a frequency synthesizer and can be switched by the standard selection (S0 and S1)].

The tracking low-pass filter is designed as a Tschebyscheff filter to guarantee sufficient suppression for the neighbouring picture carrier. An all-pass filter corrects the characteristic to obtain a flat (equivalent ripple) group delay behaviour.

Low IF differential output stage

The output amplifier consists of two identical differential operational amplifiers with a high common mode (DC) rejection ratio, to provide a constant DC voltage at the output stage. The amplified Low IF (LIF) signal is available as a differential signal with an amplitude of 2 V (p-p) and DC level of 2 V (typ.) between the output terminals of both amplifiers.

Logic control

The logic control provides an easy selection of the most common standards for Europe, USA and Japan with the two switches S0 and S1 (frequency selection different for TDA9888TS and TDA9889TS) and controls all internal standard dependent stages.

The five available tuner AGC modes can be set via the 3-state input pin S2 and R_{TOP} connection (at pin TADJ).

Internal voltage stabilizer

The band gap circuit generates a voltage of approximately 2.4 V, independent of the supply voltage and the temperature. A voltage regulator circuit, controlled by this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	I_P = 64 mA; T_{amb} = 70 °C; maximum chip temperature of 125 °C; $R_{th(j-a)}$ = maximum	–	5.5	V
$V_{i(n)}$	input voltage at pins 1 to 11, 13, 15 and 16		–	V_P	V
t_{sc}	short-circuit time to ground or V_P		–	10	s
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	ambient temperature		−20	+70	°C
V_{es}	electrostatic handling voltage for all pins	note 1	−200	+200	V
		note 2	−2500	+2500	V

Notes

1. Machine model (class B; SNW-FQ-302B): discharging a 200 pF capacitor via a 0.75 μH inductance.
2. Human body model (class 2; SNW-FQ-302A): discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	136	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; 8 MHz system; see Tables 1 or 2, CW test input signal is used for specification; $V_{i(IF)(rms)}$ = 10 mV frequency f_{IF} = 36 MHz for low IF output of 5 MHz; IF input from 50 Ω via broadband transformer 1 : 1; gain controlled amplifier adjusted to low IF differential output of 2 V (p-p); measurements taken in test circuit of Fig.11 with external 4 MHz reference signal of 140 mV (RMS); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pin V_P						
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		46	55	64	mA
P_{tot}	total power dissipation		–	275	352	mW
IF amplifier; pins IF1 and IF2; differential						
$G_{IF(max)}$	maximum conversion gain	output peak-to-peak level to input RMS level ratio	85	90	–	dB
$G_{IF(min)}$	minimum conversion gain		–	20	23	dB
$G_{IF(cr)}$	IF gain control range	see Fig.3	60	70	–	dB
$B_{IF(-3dB)(ll)}$	lower limit –3 dB IF bandwidth	note 2	–	15	–	MHz
$B_{IF(-3dB)(ul)}$	upper limit –3 dB IF bandwidth	note 2	–	80	–	MHz
$R_{i(dif)}$	differential input resistance	note 2	–	2	–	kΩ
$C_{i(dif)}$	differential input capacitance	note 2	–	3	–	pF
V_I	DC input voltage		–	1.9	–	V
Low IF output signal; pins LIF1 and LIF2; differential; see Fig.8						
$V_{o(LIF)(p-p)}$	typical low IF operating output voltage (peak-to-peak value)		–	2	–	V
$V_{clip(u)}$	upper clipping voltage level (single-ended)		2.9	–	–	V
$V_{clip(l)}$	lower clipping voltage level (single-ended)		–	–	0.6	V
$R_{o(diff)}$	output resistance (differential)	note 2	–	–	150	Ω
V_O	DC output voltage		–	2	–	V
$I_{bias(int)}$	internal DC bias current for emitter-follower (single-ended)		0.8	1	–	mA
$I_{o(source)(max)}$	maximum AC and DC output source current (single-ended)		2.5	–	–	mA
$I_{o(sink)(max)}$	maximum AC and DC output sink current (single-ended)	note 3	0.6	–	–	mA
$Z_{L(diff)}$	differential load impedance	note 2	1.7	–	–	kΩ
α_{LIF}	low IF band amplitude characteristic	0 dB at middle of band (standard independent)	–0.9	–	+0.9	dB
$t_{d(g)(LIF)}$	low IF band group delay ripple	from 1 MHz to 2 MHz	–	–	150	ns
		from 2 MHz to end of band	–	–	100	ns
α_{N-1}	low-pass filter attenuation	6 MHz band; at 11.75 MHz	15	–	–	dB
		7 MHz band; at 13.75 MHz	15	–	–	dB
		8 MHz band; at 15.75 MHz	15	–	–	dB
α_{27MHz}	low-pass filter attenuation	any band; at 27 MHz	40	50	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{N+1}	suppression of IF input frequencies below wanted band at low IF output	input frequency between 21 and 31 MHz; referenced to 36 MHz	30	35	–	dB
C/N	carrier-to-noise ratio at low IF	at Δf = 4.9 MHz; note 4a; see Fig.5	112	116	–	dBc/Hz
		at Δf = 4.9 MHz; note 4b; see Fig.5	90	100	–	dBc/Hz
α_{d3}	intermodulation at f_{LIF1} = 4.1 MHz or f_{LIF2} = 5.9 MHz	$f_{IF1} = f_{osc}$ + 4.7 MHz and $f_{IF2} = f_{osc}$ + 5.3 MHz; see Fig.6	40	–	–	dB
α_{d2}	in-band harmonics low IF = multiple of 1.31 MHz up to 7.86 MHz	$f_{IF1} = f_{osc}$ + 1.31 MHz	40	–	–	dB
$\alpha_{H(spur)}$	in-band spurious elements (1 to 9 MHz)	AC load: $Z_{L(diff)} > 1.7$ kΩ	50	–	–	dB
	out-band spurious elements (>9 MHz)		50	–	–	dB
PSRR	power supply ripple rejection [residual ripple FM, peak deviation Δf at 2 V (p-p) low IF signal]	f_{ripple} = 70 Hz; see Fig.7	–	–	5	Hz
		f_{ripple} = 1 kHz; see Fig.7	–	25	35	Hz
		f_{ripple} = 10 kHz; see Fig.7	–	1400	2000	Hz
		f_{ripple} = 100 kHz; see Fig.7	–	2700	4000	Hz
	power supply ripple rejection [residual ripple AM, modulation factor m at 2 V (p-p) low IF signal]	f_{ripple} = 70 Hz; see Fig.7	–	1.4	–	%
IF AGC control; pin AGC						
$I_{i(sink)(max)}$	maximum input sink current		–	–	2	µA
$V_{i(max)}$	maximum allowable input voltage		–	–	V_P	V
G_v	gain control voltage range		0	–	3	V
S_{AGC}	negative control steepness $\Delta G_{IF}/\Delta V_{con}$	G_v = 0.8 to 2.2 V	–	45	–	dB/V
Tuner AGC; pin TAGC, operating as current output; see Figs 3 and 4						
$V_{i(IF)(min)(p-p)}$	minimum controlled IF input signal voltage between pins IF1 and IF2 (peak-to-peak value)	R_{TOP} = 22 kΩ; $I_{TAGC(sink)}$ = 100 µA	–	81	84	dBµV
$V_{i(IF)(max)(p-p)}$	maximum controlled IF input signal voltage between pins IF1 and IF2 (peak-to-peak value)	R_{TOP} = 0 Ω; $I_{TAGC(sink)}$ = 100 µA	102	106	–	dBµV
$V_{i(IF)}/\Delta T$	variation of AGC controlled IF input voltage with temperature	R_{TOP} = 8.2 kΩ; $I_{TAGC(sink)}$ = 100 µA	–	–	0.07	dB/K
I_{sink}	sink current (tuner AGC discharge current)	V_{TAGC} = 1 V	400	500	600	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{source(1)}$	source current (tuner AGC charge current)	normal mode	0.21	0.27	0.33	µA
$I_{source(2)}$		fast mode activated by internal level detector	8	10	12	µA
$V_{sat(ul)}$	upper limit saturation voltage	pin operating as current output	V_P – 0.3	–	–	V
$V_{sat(ll)}$	lower limit saturation voltage		–	–	0.3	V
α_{TH}	level loss threshold of internal detector for activating fast AGC	0 dB corresponds to R_{TOP} alignment	6	8	10	dB
$t_{det(off)}$	fast AGC detection off time	all signal events below α_{TH}	40	60	80	ms
External tuner AGC; electronic switch operation; pin TAGC connected to pin TAGCEXT						
R_{on}	resistance between pins TAGC and TAGCEXT in operation		–	900	1200	Ω
$V_{op(I/O)}$	I/O operating voltage range		0	–	V_P	V
Tuner AGC takeover point adjust and TAGC operating mode settings; pin TADJ; see Table 3						
V_{RTOP}	alignment voltage	R_{TOP} at pin TADJ = 0 to 22 kΩ	0	–	2	V
V_{TADJ}	voltage at pin TADJ	pin open-circuit	–	3.5	–	V
R_{TOP}	resistor connected between pin TADJ and GND	for LOW: R_{TOP} at pin TADJ	–	–	25	kΩ
		for HIGH: pin open-circuit	1	–	–	MΩ
Low-pass control PLL; pin LFLP						
V_{LFLP}	loop filter operating range		1	–	3	V
K_O	VCO steepness: $\Delta f_{VCO}/\Delta V_{LFS}$	note 5	–	4	–	MHz/V
K_D	phase frequency detector steepness: $\Delta I_{LFLP}/\Delta\varphi_{FM}$		–	9	–	µA/rad
$R_{lf(int)}$	internal loop filter resistor		3.75	4.7	5.65	kΩ
$I_{sink/source}$	phase frequency detector I/O current		–	–	65	µA
Synthesizer PLL; pin LFS						
V_{LFS}	loop filter operating range		1	–	3	V
K_O	VCO steepness: $\Delta f_{VCO}/\Delta V_{LFS}$	note 5	–	25	–	MHz/V
K_D	phase frequency detector steepness: $\Delta I_{LFS}/\Delta\varphi_{FM}$		–	16	–	µA/rad
$I_{sink/source}$	phase frequency detector I/O current		–	–	100	µA
$\phi_{N(synth)}$	synthesizer phase noise performance	at 1 kHz	89	99	–	dBc/Hz
		at 10 kHz	89	97	–	dBc/Hz
		at 100 kHz	98	102	–	dBc/Hz
		at 1.4 MHz	115	119	–	dBc/Hz
α_{spur}	synthesizer spurious performance	multiple of Δf = 500 kHz	50	–	–	dBc
$I_{leak(lf)}$	loop filter leakage current	synthesizer spurious performance > 50 dBc	–	–	10	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Standard switch S0 and S1; pins S0 and S1; see Tables 1 or 2						
V_i	input voltage	for LOW	0	–	2	V
		for HIGH	2.5	–	V_P	V
$V_{fr(S0,S1)}$	free-running voltage at pin S0 or pin S1	pin open-circuit; $I_{fr(S0,S1)} < 0.1$ μA	–	3.5	–	V
R_i	input resistance		–	37	–	kΩ
Standard switch S2; pin S2; see Table 3						
V_i	input voltage	for LOW	0	–	0.8	V
		for MID	1.3	–	2	V
		for HIGH	2.5	–	V_P	V
$V_{fr(S2)}$	free-running voltage at pin S2	pin open-circuit; $I_{fr(S2)} < 0.1$ μA	–	1.65	–	V
R_i	input resistance		–	25	–	kΩ
Reference input; pin REF; note 6						
V_I	DC input voltage		2.3	2.6	2.9	V
R_i	input resistance		1.5	2	2.5	kΩ
C_i	input capacitance		–	2	–	pF
R_{xtal}	resonance resistance of crystal	operation as crystal oscillator	–	–	200	Ω
C_x	pull-up/down capacitance	note 7	depends on crystal type			pF
f_{ref}	frequency of reference signal		–	4	–	MHz
Δf_{ref}	tolerance of reference frequency	note 8	–	–	$\pm 100 \times 10^{-6}$	
$V_{ref(p-p)}$	amplitude of reference signal source (peak-to-peak value)	operation as input terminal	230	–	1100	mV
$R_{o(ref)}$	allowed output resistance of external reference source		–	–	4.7	kΩ
C_K	decoupling capacitance to external reference source	operation as input terminal	22	100	–	pF

Notes

1. Some parameters can be decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information.
3. For a higher AC load a resistor application is possible.
4. Measured without input signal but AGC adjusted corresponding to following input level
   a) 10 mV (RMS)
   b) 0.5 mV (RMS).
5. Calculation of the PLL loop filter by using following formulae, valid under the condition for the damping factor $d \geq 1.2$.

   $BL_{-3\,dB} = \frac{1}{2\pi}\frac{K_O}{n}K_D R_{LFS}$ and $d = \frac{1}{2}R_{LFS}\sqrt{\frac{K_O}{n}K_D C_{LFS}}$ with the following parameters

   K_O = VCO steepness (rad/V) or (2π Hz/V),
   K_D = phase frequency detector steepness (μA/rad),
   R_{LFS} = synthesizer loop filter serial resistor (Ω),
   C_{LFS} = synthesizer loop filter serial capacitor (F),
   BL_{-3dB} = loop filter bandwidth at −3 dB amplitude (Hz),
   d = damping factor
   n = divider factor; see Table 4.
6. The reference input at pin S2 is able to operate as a one-pin crystal oscillator as well as an input terminal with external reference signal, e.g. from the tuning system.
7. The value of C_x determines the accuracy of the resonance frequency of the crystal and depends on the crystal type.
8. The tolerance of the reference frequency determines the accuracy of the low IF. The tolerance of f_{osc} is given by

   $\Delta f_{osc} = \frac{\Delta f_{ref}}{f_{ref}} f_{osc}$ and the tolerance of f_{LIF} is given by $\Delta f_{LIF} = -\Delta f_{osc}$.

Table 1 Standard switch settings for TDA9889TS

S1	S0	$f_{IF(centre)}$ (MHz)	f_{osc} (MHz)	CHANNEL BANDWIDTH (MHz)	REGION
HIGH	HIGH	36	31	8	Europe
HIGH	LOW	36	31.5	7	Europe
LOW	HIGH	44	40	6	USA
LOW	LOW	36	32	6	Europe

Table 2 Standard switch settings for TDA9888TS

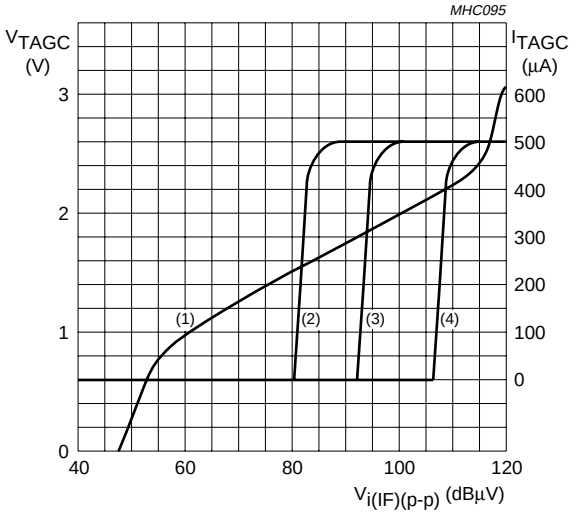
S1	S0	$f_{IF(centre)}$ (MHz)	f_{osc} (MHz)	CHANNEL BANDWIDTH (MHz)	REGION
HIGH	HIGH	36	31	8	Europe
HIGH	LOW	36	31.5	7	Europe
LOW	HIGH	44	40	6	USA
LOW	LOW	57	53	6	Japan

Table 3 AGC mode settings

S2	R_{TOP}	FUNCTION (PIN TADJ)
LOW	connected	all currents off; voltage from pin TAGCEXT switched to pin TAGC
MID		charge currents disabled; discharge current enabled
HIGH		all charge and discharge currents enabled
MID/HIGH	open-circuit	all currents off; pin TAGC high-ohmic
LOW		all currents off; voltage from pin TAGCEXT switched to pin TAGC

Table 4 Synthesizer PLL loop filter dimensions for different standards; see note 5 of Chapter “Characteristics”

$f_{IF(centre)}$ (MHz)	f_{osc} (MHz)	n	BL_{-3dB} (kHz)	d	R_{LFS} (kΩ)	C_{LFS} (nF)	$C_{P(LFS)}$ (pF)
36	31	62	36.1	1.22	5.6	4.7	22
	31.5	63	35.6	1.21			
	32	64	35	1.20			
44	40	80	34	1.31	6.8		18
57	53	106	34.4	1.52	9.1		15



(1) IF AGC voltage.
(2) I_{tuner}; R_{TOP} = 8.2 kΩ.
(3) I_{tuner}; R_{TOP} = 0 Ω.
(4) I_{tuner}; R_{TOP} = 0 Ω.

Fig.3 Typical IF and tuner AGC characteristic.

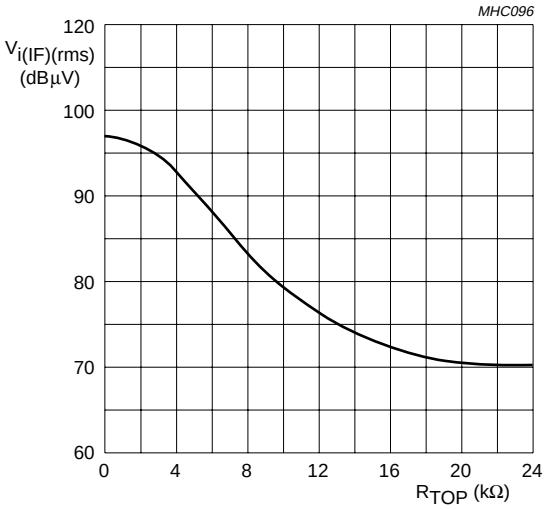


Fig.4 Typical tuner takeover point as a function of R_{TOP}.

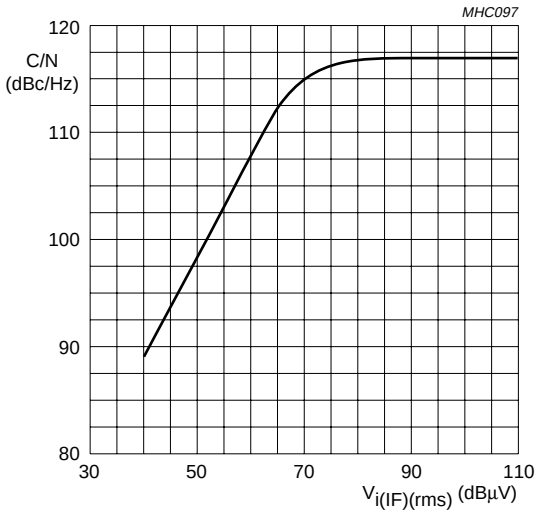


Fig.5 Typical C/N ratio as a function of IF input voltage.

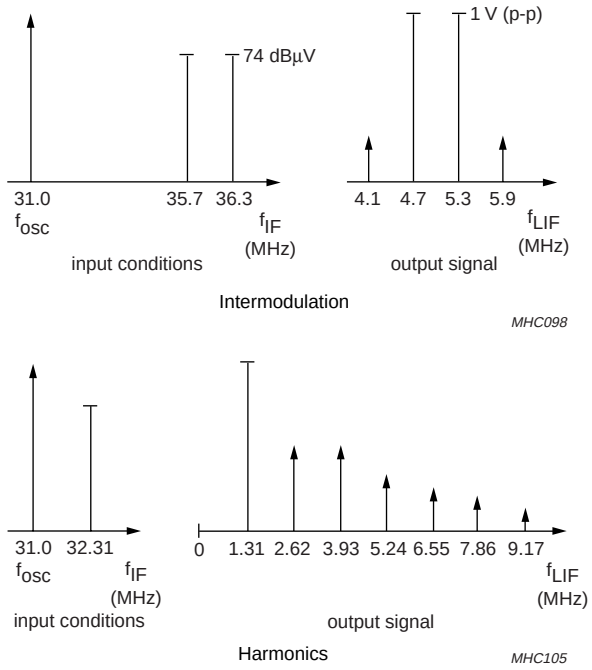


Fig.6 Intermodulation and harmonics.

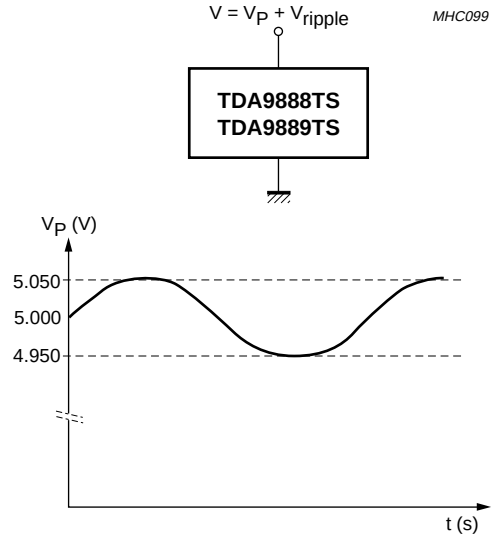
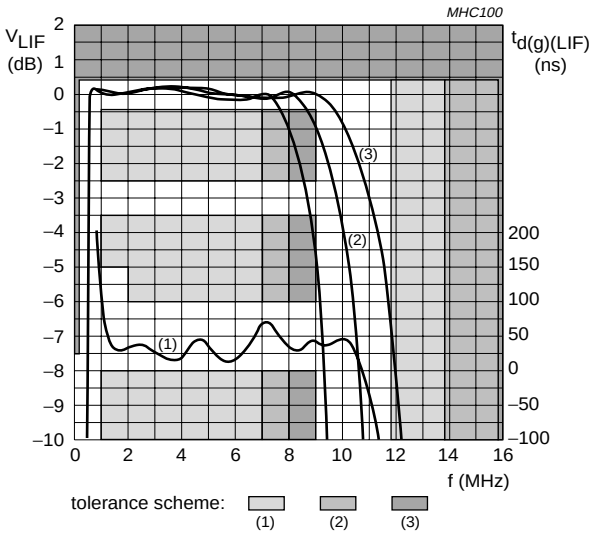
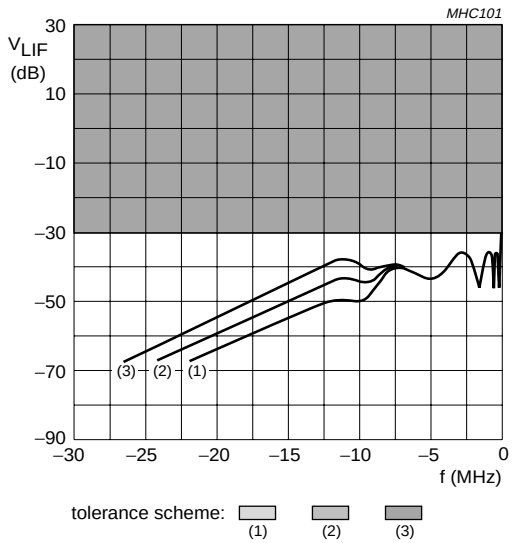


Fig.7 Ripple rejection condition.



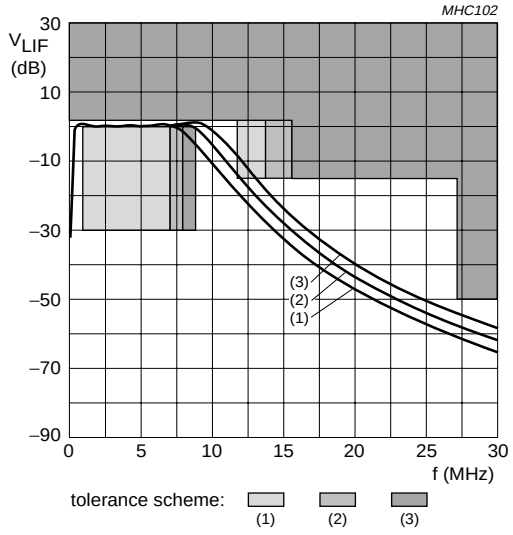
(1) Channel bandwidth = 6 MHz.
(2) Channel bandwidth = 7 MHz.
(3) Channel bandwidth = 8 MHz.

Fig.8 Detailed low IF amplitude and group delay pass band tolerance scheme.



(1) Channel bandwidth = 6 MHz.
(2) Channel bandwidth = 7 MHz.
(3) Channel bandwidth = 8 MHz.

Fig.9 Low IF amplitude stop band tolerance scheme.



(1) Channel bandwidth = 6 MHz.
(2) Channel bandwidth = 7 MHz.
(3) Channel bandwidth = 8 MHz.

Fig.10 Low IF amplitude pass band tolerance scheme.

TEST AND APPLICATION INFORMATION

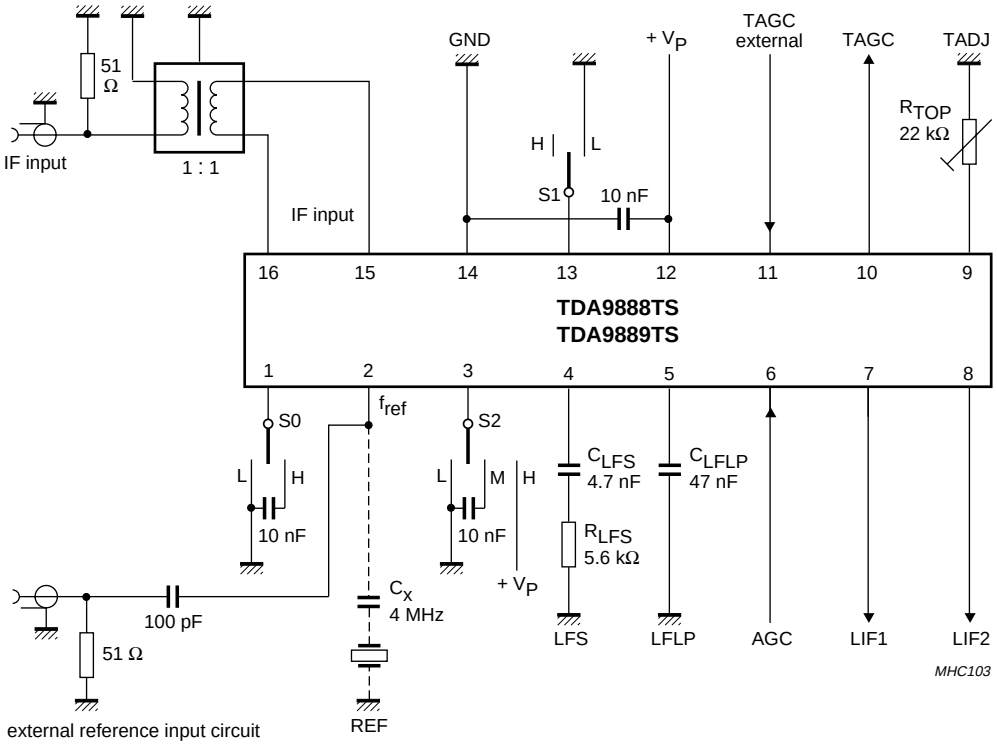
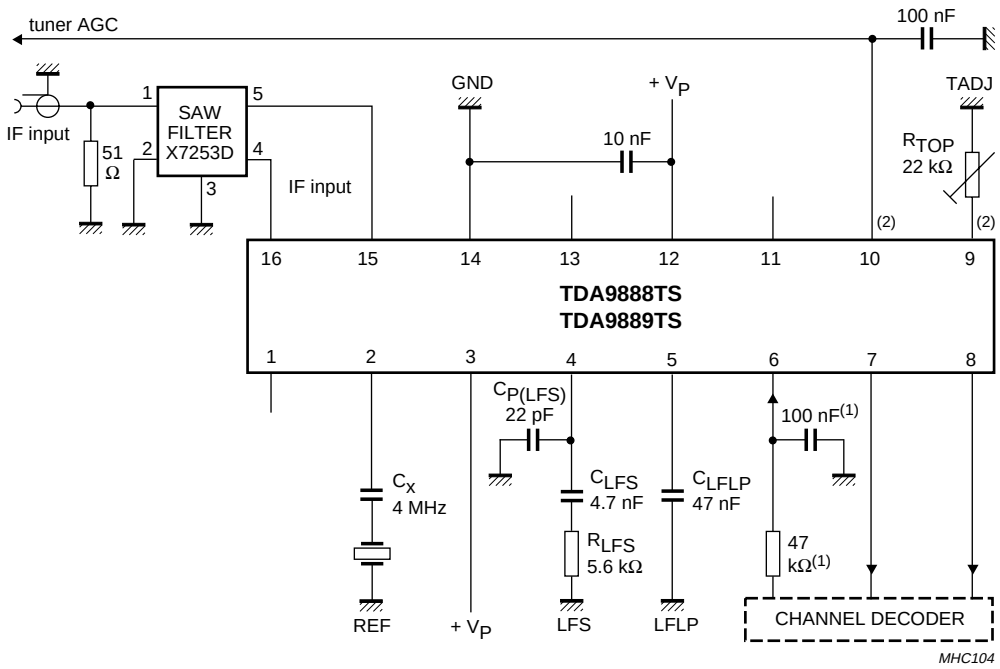


Fig.11 Test circuit.



f_{IF} = 36 MHz; channel bandwidth = 8 MHz; external AGC from channel decoder; inclusive narrow band tuner AGC.

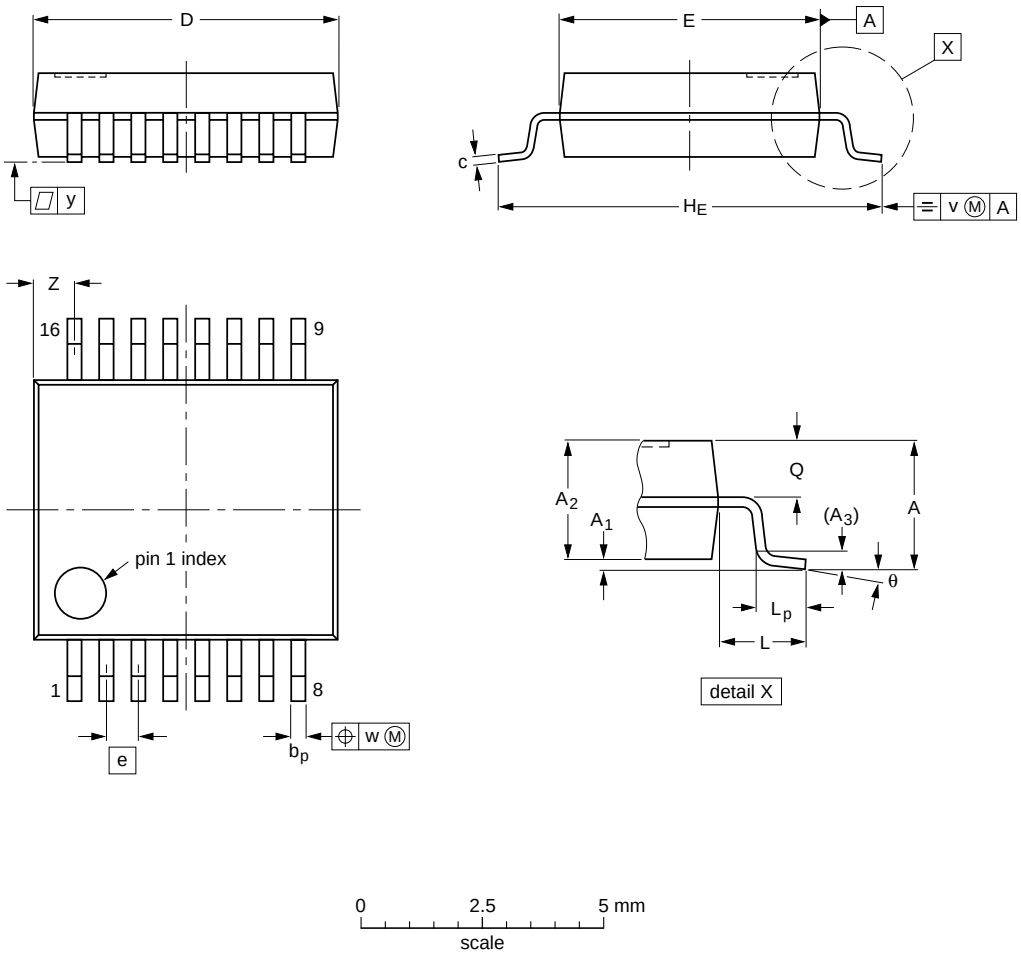
(1) Depends on channel decoder.

(2) Open-pin if tuner AGC is not needed.

Fig.12 Application circuit.

PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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